wherein said memory thin film transistor comprises:

a first semiconductor active layer over an insulating substrate;

a first insulating film;

a floating gate electrode;

a second insulating film;

a control gate electrode;

a wiring for connecting the control gate electrode with a first signal line,

wherein said switching thin film transistor comprises:

a second semiconductor active layer over the insulating substrate;

a gate insulating film;

a gate electrode connected to a second signal line,

wherein the memory thin film transistor and the switching thin film transistor are integrally formed over the insulating substrate,

wherein the first semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island,

wherein a first thickness of the first semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second semiconductor active layer of the switching thin film transistor,

wherein the first semiconductor active layer of the memory thin film transistor is connected to a third signal line,

wherein the second semiconductor active layer of the switching thin film transistor is connected to a fourth signal line,

wherein the second signal line is formed between the semiconductor active layers and the first signal line,

wherein the first signal line and the second signal line are perpendicular to the third signal line and the fourth signal line,

wherein the floating gate electrode of the memory thin film transistor, the gate electrode of the switching thin film transistor, the first signal line and the second signal line are formed of a same layer,

wherein the wiring of the memory thin film transistor, the third signal line and the fourth signal line are formed of a same layer, and

wherein at least two of the memory cells adjacent to each other share the fourth signal line therebetween.

3. (Twice Amended) A nonvolatile memory comprising:

a memory cell array including a plurality of memory cells being formed in a matrix, each of the memory cells including a memory thin film transistor and a switching thin film transistor,

wherein said memory thin film transistor comprises:

a first semiconductor active layer over an insulating substrate;

a first insulating film;

a floating gate electrode;

a second insulating film;

a control gate electrode;

a wiring for connecting the control gate electrode with a first signal line,

wherein said switching thin film transistor comprises:

a second semiconductor active layer over the insulating substrate;

a gate insulating film;

a gate electrode connected to a second signal line,

wherein the memory thin film transistor and the switching thin film transistor are integrally formed over the insulating substrate,

wherein the first semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island,

wherein a first thickness of the first semiconductor active layer of the memory thin film transistor is in a range of 1-100 nm while a second thickness of the second semiconductor active layer of the switching thin film transistor is in a range of 1-150 nm,

wherein the first semiconductor active layer of the memory thin film transistor is connected to a third signal line,

wherein the second semiconductor active layer of the switching thin film transistor is connected to a fourth signal line,

wherein the second signal line is formed between the semiconductor active layers and the first signal line,

wherein the first signal line and the second signal line are perpendicular to the third signal line and the fourth signal line,

wherein the floating gate electrode of the memory thin film transistor, the gate electrode of the switching thin film transistor, the first signal line and the second signal line are formed of a same layer,

C2 cont

wherein the wiring of the memory thin film transistor, the third signal line and the fourth signal line are formed of a same layer, and

wherein at least two of the memory cells adjacent to each other share the fourth signal line therebetween.

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43. (Amended) A nonvolatile memory comprising:

a memory cell array including a plurality of memory cells being formed in a matrix, each of the memory cells including a memory thin film transistor and a switching thin film transistor,

wherein said memory thin film transistor comprises:

C3

a first semiconductor active layer over an insulating substrate;

a first insulating film;

a floating gate electrode;

a second insulating film;

a control gate electrode,

wherein said switching thin film transistor comprises:

a second semiconductor active layer over the insulating substrate;

a gate insulating film; and

a gate electrode connected to a second signal line,

wherein the memory thin film transistor and the switching thin film transistor are integrally formed over the insulating substrate,

wherein the first semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island,

wherein a first thickness of the first semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second semiconductor active layer of the switching thin film transistor,

wherein the control gate electrode of the memory thin film transistor is connected to the first signal line,

wherein the first semiconductor active layer of the memory thin film transistor is connected to a third signal line,

wherein the second semiconductor active layer of the switching thin film transistor is connected to a fourth signal line,

wherein the second signal line is formed between the semiconductor active layers and the first signal line,

wherein the first signal line and the second signal line are perpendicular to the third signal line and the fourth signal line,

wherein the floating gate electrode of the memory thin film transistor, the gate electrode of the switching thin film transistor, the first signal line and the second signal line are formed of a same layer,

wherein control gate electrode of the memory thin film transistor, the third signal line and the fourth signal line are formed of a same layer, and

C3 cont

wherein at least two of the memory cells adjacent to each other share the fourth signal line therebetween.

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45. (Amended) A nonvolatile memory comprising:

a memory cell array including a plurality of memory cells being formed in a matrix, each of the memory cells including a memory thin film transistor and a switching thin film transistor,

wherein said memory thin film transistor comprises:

C4

a first semiconductor active layer over an insulating substrate;

a first insulating film;

a floating gate electrode;

a second insulating film;

a control gate electrode,

wherein said switching thin film transistor comprises:

a second semiconductor active layer over the insulating substrate;

a gate insulating film; and

a gate electrode connected to a second signal line,

wherein the memory thin film transistor and the switching thin film transistor are integrally formed over the insulating substrate,

wherein the first semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island,

wherein a first thickness of the first semiconductor active layer of the memory thin film transistor is in a range of 1-100 nm while a second thickness of the second semiconductor active layer of the switching thin film transistor is in a range of 1-150 nm,

wherein the control gate electrode of the memory thin film transistor is connected to the first signal line,

wherein the first semiconductor active layer of the memory thin film transistor is connected to a third signal line,

C4 cont.

wherein the second semiconductor active layer of the switching thin film transistor is connected to a fourth signal line,

wherein the second signal line is formed between the semiconductor active layers and the first signal line,

wherein the first signal line and the second signal line are perpendicular to the third signal line and the fourth signal line,

wherein the floating gate electrode of the memory thin film transistor, the gate electrode of the switching thin film transistor, the first signal line and the second signal line are formed of a same layer,

wherein the control gate electrode of the memory thin film transistor, the third signal line and the fourth signal line are formed of a same layer, and

wherein at least two of the memory cells adjacent to each other share the fourth signal line therebetween.

60. (Amended) A semiconductor device comprising:

a memory cell array comprising a plurality of memory cells formed over a substrate in a matrix, each of the memory cells comprising:

a memory thin film transistor comprising a first semiconductor active layer formed on an insulating surface, a floating gate electrode and a first control gate electrode; and

a switching thin film transistor electrically connected to the memory thin film transistor, said switching thin film transistor comprising a second semiconductor active layer formed on the insulating surface and a second gate electrode,

a first signal line and a second signal line extending in parallel in a first direction over the substrate, said first signal line being electrically connected to the control gate electrode of the memory thin film transistor and said second signal line being electrically connected to the second gate electrode of the switching thin film transistor;

an interlayer insulating film formed over the first signal line and the second signal line;

a third signal line and a fourth signal line formed over the interlayer insulating film and extending in parallel in a second direction orthogonal to the first direction said third signal line being electrically connected to one of source and drain regions of the memory thin film transistor and said fourth signal line being electrically connected to one of source and drain regions of the switching thin film transistor; and

a conductive film formed over the interlayer insulating film, said conductive film electrically connecting said first signal line and said control gate electrode of the memory thin film transistor,

wherein the first semiconductor active layer and the second semiconductor active layer of one of the memory cells are formed in a common semiconductor island,

C5 cont.

wherein the floating gate electrode of the memory thin film transistor, the second gate electrode of the switching thin film transistor, and the first and second signal lines are formed of a same layer,

wherein the third and fourth signal lines and said conductive film are formed of a same layer,

wherein said conductive film extends across the second signal line, and

wherein at least two of the memory cells adjacent to each other share the fourth signal line therebetween.

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66. (Amended) A semiconductor device comprising:

a display portion comprising a plurality of pixel thin film transistors over a substrate;

C4

a memory cell array comprising a plurality of memory cells formed over a substrate in a matrix, each of the memory cells comprising:

a memory thin film transistor comprising a first semiconductor active layer formed on an insulating surface, a floating gate electrode and a first control gate electrode; and

a switching thin film transistor electrically connected to the memory thin film transistor, said switching thin film transistor comprising a second semiconductor active layer formed on the insulating surface and a second gate electrode;

a first signal line and a second signal line extending in parallel in a first direction over the substrate, said first signal line being electrically connected to the control gate electrode of the memory thin film transistor and said second signal line being electrically connected to the second gate electrode of the switching thin film transistor;

an interlayer insulating film formed over the first signal line and the second signal line;

C4

a third signal line and a fourth signal line formed over the interlayer insulating film and extending in parallel in a second direction orthogonal to the first direction, said third signal line being electrically connected to one of source and drain regions of the memory thin film transistor and said fourth signal line being electrically connected to one of source and drain regions of the switching thin film transistor; and

a conductive film formed over the interlayer insulating film and electrically connecting said first signal line and said control gate electrode of the memory thin film transistor,

wherein the first semiconductor active layer and the second semiconductor active layer of one of the memory cells are formed in a common semiconductor island,

wherein the floating gate electrode of the memory thin film transistor, the second gate electrode of the switching thin film transistor, and the first and second signal lines are formed of a same layer,

wherein the third and fourth signal lines and said conductive film are formed of a same layer,

wherein said conductive film extends across the second signal line, and

wherein at least two of the memory cells adjacent to each other share the fourth signal line therebetween.